CLAIMS

1. A phase lock loop (PLL) circuit for receiving a burst signal including a repeated preamble sequence and a data sequence; the circuit comprising:

a maximum likelihood sequence estimator (MLSE) and means for determining the phase difference between a signal at the output of the MLSE and a corresponding delayed signal at the input of the MLSE;

phase rotating means for rotating the phase of said burst signal dependent on said phase difference, the output of said means being coupled to the MLSE input;

wherein the phase determining means is further arranged to determine the phase difference between a non-delayed signal at the MLSE input and a stored preamble sequence signal.

2. A circuit according to claim 1 wherein the phase determining means is arranged to determine the phase difference between said preamble memory and said non-delayed MLSE input when said signal is carrying said preamble sequence; and wherein said phase determining means is arranged to determine the phase difference between said MLSE output and said delayed MLSE input when said signal is carrying said data sequence.

3. A circuit according to claim 1 wherein said MLSE is an Ungerbroeck's type MLSE.

4. A circuit according to claim 1 wherein the phase determining means comprises a phase detector and a switching means;

the phase detector having a first input switchably coupled to the MLSE input and a delay means coupled to the MLSE input, the delay means for delaying the MLSE input signal by a delay time corresponding to the processing delay of the MLSE; and a second input switchably coupled to the MLSE output and a preamble memory means which stores said preamble sequence signal;

processing means arranged to determine the phase difference between the first and second inputs, the processing means arranged to determine the imaginary part of dividing the second input by the first input; said part corresponding to the phase difference.

5. A circuit according to claim 1 wherein the phase rotating means comprises a mixer; and a second order filter and a NCO are coupled between the phase detector output and said mixer.

6. A receiver for receiving a burst signal including a repeated preamble sequence and a data sequence; the receiver comprising a PLL circuit according to claim 1.

7. A receiver according to claim 6 further comprising a preamble frequency offset estimator having:

means for differentially multiplying a sample of a first said preamble sequence with a corresponding sample of a second said preamble sequence;

means for determining a phase rotation angle dependent on said difference and which angle is indicative of said estimate.

8. A receiver according to claim 7 further comprising a frequency shifter which shifts the phase of said received signal by said phase rotation angle.

9. A carrier recovery architecture for receiving a burst signal including a repeated training sequence and a data sequence; the architecture comprising:

a PLL having a mixer which receives a signal, an MLSE having an input coupled to the mixer, and a phase detector, the phase detector arranged to determine the phase difference between a signal at an output of the MLSE and a corresponding delayed signal at the MLSE input ;

the PLL further having mixer input means which is arranged to provide a rotating signal to the mixer in order to adjust the frequency of the received signal which the mixer outputs to the MLSE, said rotating signal being dependent on said phase difference;

wherein the phase detector is arranged to be switch-able between said MLSE output and a training sequence memory, and between said MLSE delayed input and a non-delayed MLSE input.

10. A phase detector having an input coupled to the output of a maximum likelihood sequence estimator (MLSE) and a second input coupled to the input of said MLSE; the detector comprising:

delay means for delaying the second input signal by a delay time corresponding to the processing delay of the MLSE;

processing means arranged to determine the phase difference between the first and delayed second inputs;

the processing means arranged to determine the imaginary part of the result of dividing the second input by the first input; said part corresponding to the phase difference.

11. A detector according to claim 9 further comprising switching means arranged to switch said second input to said MLSE input (non-delayed) and to switch said first input to a sequence memory means.